REMARKS

This paper is presented in response to the Office Action. By this paper, claims 1, 2, 4 and 11 are amended, claims 17-21 are canceled, and new claims 22-40 are added. Claims 1-16 and 22-40 are now pending in this application as a result of the aforementioned cancellations and new claims.

Reconsideration of the application is respectfully requested in view of the following remarks. For the convenience and reference of the Examiner, the remarks are presented in the order in which the corresponding issues were raised in the Office Action.

I. General Considerations

Applicant notes that the remarks and amendments presented herein have been made merely to clarify the claimed embodiments from elements purported by the Examiner to be taught by the cited references. Such remarks, or a lack of remarks, and amendments are not intended to constitute, and should not be construed as, an acquiescence, on the part of the Applicant: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case. Applicant reserves the right to challenge the purported teaching and prior art status of the cited references at any appropriate time.

In addition, the remarks herein do not constitute, nor are they intended to be, an exhaustive enumeration of the distinctions between any cited references and the claimed invention. Rather, the distinctions identified and discussed herein are presented solely by way of example. Consistent with the foregoing, the discussion herein is not intended, and should not be construed, to prejudice or foreclose contemporaneous or future consideration, by the Applicant, of additional or alternative distinctions between the claims of the present application and the references cited by the Examiner, and/or the merits of additional or alternative arguments.

II. Claim Objections

The Examiner has objected to claims 1, 4 and 11 because of various asserted informalities. In view of the amendments herein to claims 1, 4 and 11, Applicant submits that the objection has been overcome and should be withdrawn.

III. Claim Rejections Under 35 U.S.C. §102

Applicant respectfully notes that a claim is anticipated under 35 U.S.C. § 102(a), (b), or (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Further, the identical invention must be shown in as complete detail as is contained in the claim. Finally, the elements must be arranged as required by the claim. *Manual of Patent Examining Procedure ("MPEP") § 2131.*

The Examiner has rejected claims 1-2, 4, 8-9, 11, 13, 17 and 21 under 35 U.S.C. § 102(b) as being anticipated by *A Novel Transmitter/Receiver Switching Circuit Configuration for High-Performance LD Transceiver in Subscriber Loop*, Kimura et al., Journal of Lightwave Technology, Vol. 14, No. 7, July 1996 ("*Kimura*"). Applicant disagrees with the contentions of the Examiner however and submits that for at least the reasons outlined below, the rejection of those claims should be withdrawn.

a. claims 1-2

In rejecting the claims, the Examiner has asserted that *Kimura* discloses "... a plurality of external test pins coupled to the oxide laser diode wherein the test pins are adapted to be connected to external testing equipment (figures 12 and 14(b))." Applicant respectfully disagrees.

Particularly, Applicant has reviewed Figure 12 of *Kimura* and has been unable to find any reference in that Figure either to "test pins" or to "external testing equipment," configured and arranged as required by claim 1. Instead, the laser diode LD of Figure 12 appears to be connected only to a "preamp," a "laser driver," "switch 1," "switch 2" and "power supply V_{dd1}." In view of the foregoing, Applicant respectfully requests the assistance of the Examiner in specifically identifying which component(s) of *Kimura* that the Examiner believes to constitute the purported "test pins" in Figure 12 of *Kimura*.

Applicant has also reviewed Figure 14(b) of *Kimura*, cited by the Examiner in support of the rejection of claim 1, and has similarly been unable to find any reference in that Figure either to "test pins" or to "external testing equipment," configured and arranged as required by claim 1. For example, while Figure 14(b) does refer to an "LD module," that Figure does not appear to indicate that any pins are connected to that "LD module," much less "test pins" as required by claim 1. In fact, the only pins or connections that are apparent in Figure 14(b) are the leads of the "Preamp IC." However, claim 1 requires that the "test pins" be connected to the "laser diode," not to a "Preamp IC." In view of the foregoing, Applicant respectfully requests the assistance of the Examiner in specifically identifying which

component(s) of *Kimura* that the Examiner believes to constitute the purported "test pins" in Figure 14(b) of *Kimura*.

With the foregoing in view, Applicant respectfully submits that the Examiner has not established that *Kimura* anticipates claim 1, at least because the Examiner has not established that each and every element as set forth in claim 1 is found in *Kimura*, and because the Examiner has not established that the identical invention is shown in *Kimura* in as complete detail as is contained in claim 1. Applicant thus submits that the rejection of claim 1, as well as the rejection of corresponding dependent claim 2, should be withdrawn.

b. claims 4 and 8-9

In the rejection of claims 4 and 8-9, the Examiner has asserted that *Kimura* discloses "... a microprocessor coupled to the laser driver (page 1650, 2nd col., lines 1-8; figures 14(b) and 15)." Applicant respectfully disagrees.

For example, Applicant has reviewed the cited passage, namely, page 1650, 2nd col., lines 1-8, and has been unable to locate any reference to a "microprocessor," much less a microprocessor configured and arranged as required by claim 4. For the reference of the Examiner, the cited passage is reproduced below:

> ... LD transceiver module. Fig. 15 shows a photograph of LD transceiver module with new switching circuit and high isolation substrate. Overall module size is 90 x 90 mm^2. In the LD transceiver modules, we used a low noise preamplifier with I_{eq} = 1.0pA $[(Hz)^{1/2}]$, a CMOS gain control amplifier (GCA) [10] as the electrical receiver circuits and low-parasitic capacitance, high sensitivity LD (LEAD diode) module [6] with S = 0.4 A/W as the optical device.

Clearly, there is no reference in this passage to a "microprocessor" such as is recited in claim 4.

Similarly, a review of Figure 14(b) of *Kimura* indicates that a number of components are disclosed there, namely, an "LD driver," "Preamp IC," "Transistor Qc," "cathode," "anode," "LD module," "Transistor Qa," "Gain Control Amp" and "LD Driver." However, Figure 14(b) makes no apparent reference to any "microprocessor," much less a microprocessor configured and arranged as required by claim 4. In fact, *Kimura* characterizes Figure 14 by stating simply that "Fig. 14 shows the LD transceiver substrate configuration around the preamplifier and the output wave forms of preamplifier simulated by the FD-TD method." *Page 1650, col. 1, lines 5-7.*

Applicant respectfully submits that Figure 15 of *Kimura* is likewise an inadequate basis for the rejection made by the Examiner. Particularly, Applicant submits that the quality of the image of Figure

15 in Applicant's copy of *Kimura* is so poor that it is difficult, if not impossible, to reach a firm conclusion that such Figure discloses any particular component, much less a "microprocessor." Further, and as noted above, the description of Figure 15 in *Kimura* makes no reference whatsoever to a "microprocessor." Finally, even if it is assumed, strictly for the sake of argument, that Figure 15 of *Kimura* discloses a microprocessor, Applicant respectfully submits that it would simply be impossible to determine, by mere inspection of Figure 15, whether any such microprocessor is "adapted to collect periodic operating characteristics of the laser diode and to compare the periodic operating characteristics of the laser diode to the reference operating characteristics of the laser diode," as claim 4 requires.

Finally, the Examiner has also asserted that *Kimura* discloses "wherein the microprocessor is adapted to collect periodic operating characteristics of the laser diode and to compare the periodic operating characteristics of the laser diode to the reference operating characteristics of the laser diode (page 1647, 2nd col., last paragraph; figures 5 and 12)." Again however, Applicant respectfully submits that the reliance of the Examiner on *Kimura* is misplaced.

For example, while the passage of *Kimura* cited by the Examiner states in part that "This experimental result shows the effectiveness of the DCCT. By setting the capacitance and resistance parameters of reference element more accurately, the DCCT could yield better performance. We believe that the DCCT will be very effective for realizing an LD transceiver module because the optimization of bias-voltage and time, which is needed in the FDT, is not necessary in the DCCT and its module configuration is much simpler," that passage is inadequate to support the rejection of the claims for a variety of reasons. For example, the passage does not indicate that any of the processes recited there are performed by a microprocessor that comprises an element of a transceiver, as claim 4 clearly requires.

In rejecting claims 4 and 8-9, the Examiner has further asserted that *Kimura* discloses "memory coupled to the microprocessor, the memory comprising a reference operating characteristic of the laser diode (page 1644, 2nd col., lines 1-3; page 1650, 2nd col., lines 1-8; figure 12)." However, a review of these portions of *Kimura* cited by the Examiner reveals that the characterization of such portions advanced by the Examiner is not well taken.

For example, the passage at page 1644 of *Kimura* cited by the Examiner reads "To suppress the signal drift induced by the discharge current of a LD, we introduce two methods for suppressing signal drift. The first method, which is new, is to cancel the discharge current effect by using the discharge current as the differential preamplifier reference." Applicant respectfully submits that it is clear that, contrary to the assertion of the Examiner, the foregoing passage makes no reference to a

"microprocessor" [of a transceiver] or a "memory [of a transceiver] coupled to the microprocessor, the memory comprising a reference operating characteristic of the laser diode," as required by claim 4. The other passages cited by the Examiner are likewise unavailing.

Particularly, page 1650, 2nd col., lines 1-8 of *Kimura* (reproduced above) makes no reference to either a microprocessor or a memory, much less a microprocessor and memory configured and arranged as required by claim 4. Finally, Figure 12 of *Kimura* fails to disclose any microprocessor or memory, much less a microprocessor and memory configured and arranged as required by claim 4.

In view of the foregoing discussion, Applicant respectfully requests the assistance of the Examiner in specifically identifying which particular components of *Kimura* the Examiner believes to correspond to the elements of claim 4.

With the foregoing in view, Applicant respectfully submits that the Examiner has not established that *Kimura* anticipates claim 4, at least because the Examiner has not established that each and every element as set forth in claim 4 is found in *Kimura*, and because the Examiner has not established that the identical invention is shown in *Kimura* in as complete detail as is contained in claim 4. Applicant thus submits that the rejection of claim 4, as well as the rejection of corresponding dependent claims 8-9, should be withdrawn.

c. claims 11 and 13

Similar to claim 4, claim 11 requires "a microprocessor coupled to the laser driver ... memory coupled to the microprocessor ... wherein the microprocessor is adapted to: collect periodic operating characteristics of the laser diode ..." In connection with the foregoing, Applicant notes that the discussion of claim 4 at **III.b.** above is germane as well to the rejection of claims 11-13 and the attention of the Examiner is accordingly directed to such discussion. For at least the reasons outlined in that discussion, Applicant respectfully submits that the Examiner has not established that *Kimura* anticipates claims 11-13 and Applicant thus further submits that the rejection of those claims should be withdrawn.

d. claims 17-21

In view of the cancellation herein of claims 17-21, Applicant respectfully submits that the rejection of those claims has been rendered moot and should accordingly be withdrawn.

IV. Claim Rejections Under 35 U.S.C. §103(a)

Applicant respectfully notes at the outset that in order to establish a *prima facie* case of obviousness, it is the burden of the Examiner to demonstrate that three criteria are met: first, there must be some

suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143.

The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over *Kimura* as applied to claim 1, and further in view of US 6,802,654 to Roberts et al. ("*Roberts*"). Applicant disagrees with the contentions of the Examiner and submits that for at least the reasons outlined below, the rejection of claim 3 should be withdrawn.

By virtue of its dependence from claim 1, claim 3 requires, among other things, "a plurality of external test pins coupled to the oxide laser diode wherein the test pins are adapted to be connected to external testing equipment." As noted at **III.a.** above however, the Examiner has not established that this limitation is taught or suggested by *Kimura*, or any other reference, in combination with the other limitations of claim 1. Applicant thus submits that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 3, at least because even if the references are combined in the purportedly obvious fashion, the resulting combination fails to include all the limitations of claim 3. Applicant further respectfully submits that the rejection of claim 3 should accordingly be withdrawn.

V. Allowable Subject Matter

The Examiner has indicated that claims 5-7, 10, 12, 14-16 and 18-20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In light of the discussion herein however, Applicant respectfully declines to make such claim amendments at this time.

VI. New Claims 22-40

a. claims 22-27

By this paper, Applicant has added new dependent claims 22-27, each of which depends from claim 4. Inasmuch as claim 4 is believed to be in allowable condition, for at least the reasons set forth herein, Applicant respectfully submits that new dependent claims 22-27 are likewise in allowable condition.

b. claims 28-40

Applicant respectfully submits that, consistent with the discussion presented herein, new claims 28-40, each of which is directed to a method for screening optical transceiver modules for electrostatic discharge damage that requires, among other things, setting a fault flag if damage to the laser diode is discovered, are patentably distinct from the methods and processes purported by the Examiner to be disclosed in the references that the Examiner has cited. In this regard, Applicant notes that the Examiner has conceded that "the reason for allowance of ... claim 14 ... is the inclusion of setting a fault flag when damage to the diode is discovered ..."

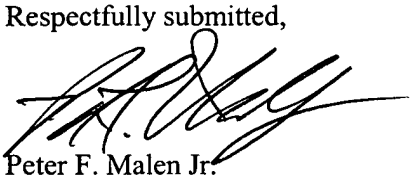
In this connection, Applicant respectfully notes that reference to the aforementioned exemplary limitation is not intended, nor should it be construed, to be either an admission or assertion by the Applicant that patentability of Applicant's new claims, or any other claims, hinges on the presence of such limitations. Rather, Applicant submits that each of the now pending claims, considered in its respective entirety, patentably distinguishes over the reference cited by the Examiner.

CONCLUSION

In view of the remarks submitted herein, Applicant respectfully submits that each of the pending claims 1-16 and 22-40 is in condition for immediate allowance. Therefore, reconsideration of the rejections is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that could be clarified in a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 24TH day of October, 2005.

Respectfully submitted,



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